**SPI INTERFACE DESCRIPTION**

Control:

The Module shall support both slave and master modes. In both modes the module input and output ports will be assigned via tristate buffers. When cpha is low the Shift Register will activate on the rising edge of SCK\_O, when cpha is high it shall activate on the falling edge of SCK\_O. When lsb\_signal is high the shift shall be a bit shift right, when it is low the shift shall be a bit shift left. An internal counter shall be used to hold the current bit position. When the internal count reaches [C\_NUM\_TRANSFER\_BITS – 1] the value in the shift register shall be written into the RX Fifo, immediately followed by the value from the TX fifo being read into the shift register. When cpol is set the SCK\_O shall be inverted. When loopback\_en is set the MOSI and MISO lines shall be shortened. When spi\_system\_en is reset the module will be disabled.

Slave Mode:

Slave mode shall initialize on the module when SPISEL\_I is reset or when spi\_master\_en is reset. Slave\_mode\_select shall be set when SPISEL\_I is set or when spi\_master\_en is set. The carry in for the shift register shall be MOSI\_I. The carry out on the shift register will be MISO\_O.

Master Mode:

BRG shall be active when module is in master mode. SCK\_O shall be set to the resultant signal of SCK\_I divided by C\_SCK\_RATIO. When manuel\_ss\_en is high the SS(N) bus shall output the value in the SPISSR. When manuel\_ss\_en is low then the SS(N) bus shall iterate through the SS bits. The carry in to the shift register shall be MISO\_I. The carry out for the shift register shall be connected to MOSI\_O when master\_inhibit is low.